

Master Program in Computer Science and Networking
High Performance Computing

2012-13

Homework 7

Exercises and questions on Part 2

in addition to exercises and questions of Sections 9 and 10

Questions 1

- a) Prove that the ideal service time of the Processing Element Interface unit (W) in a multiprocessor architecture is equal to one clock cycle. *Comment:* the proof must be done by taking all the possible functionalities of W into account.
- b) Prove that the minimum ideal service time of a switch unit in a limited degree interconnection network is equal to the clock cycle divided by the network degree. *Comment:* the evaluation must be done in the general case of maximum message load, which *does not* mean that the message headers on all the input links are received exactly during the same clock cycle.
- c) Explain why the presence of the Communication Unit (UC) is necessary in order to implement interprocessor communications in multiprocessor architectures. *Comment:* the question is *not* which functionalities are performed by UC.
- d) Explain the deterministic routing algorithm for a generalized fat tree used for shared memory access in
 - i. a SMP architecture
 - ii. a NUMA architecture.
- e) Find the base memory access latency in a NUMA architecture with k-ary 2-cube interconnect, in the following cases:
 - i. Source and destination nodes belong to the same ring;
 - ii. Source and destination nodes belong to the most distant rings.
- f) Discuss good NUMA mappings of typical parallel program schemes according to the basic paradigms studied in Part 1: farm, map, an example of static fixed stencil, an example of static variable stencil, map + reduce.
- g) Explain the following sentence: "in a multiprocessor architecture the interprocess communication runtime support is implemented using a combination of global environment mechanisms and local environment mechanisms". Moreover: why not using local environment mechanisms only?
- h) Describe the detailed implementation of the busy waiting situation in an exclusive mapping approach.
- i) Explain the following sentence: "lock-unlock operations are not only used for mutual exclusion on shared memory data structures".
- j) Define clearly the meaning of "indivisible sequence of memory accesses", and explain the difference between an indivisible sequence of memory accesses and a lock section.
- k) Describe the detailed implementation of automatic cache coherence with invalidation according to the directory-based approach..
- l) Describe the detailed implementation of a zero-copy communication using the communication processor.
- m) Explain in which way the basic I/O mechanisms (Memory Mapped I/O and DMA) are exploited in the implementation of interprocess communication in multicomputer architectures.

Question 2

- a) Implement, and evaluate the completion time of, one or more parallel stream-based versions of the matrix-vector product, with $M = 10^3$ and interarrival time equal to $M^2 \tau/2$.

The firmware architecture is a multiprocessor with the following characteristics:

- NUMA all-cache architecture;
- $N = 64$ processing elements;
- each chip contains a processing elements except the local memory;
- binary generalized fat tree interconnection network, with wormhole flow control, 32-bit links and flits, single-buffering rdy-ack communication, and link transmission latency equal to 5τ ;
- D-RISC scalar pipeline CPU, with time slot equal to 2τ , and parallel-pipelined Execution Unit. The on-chip cache hierarchy contains the primary cache only, with capacity 16K (instructions) + 32K (data), 8-word block, associative, write-through;
- shared memory macro-modules, 8 interleaved modules with 16G capacity and clock cycle equal to 20τ ;
- communication processor and zero-copy communication;
- exclusive mapping;
- automatic cache coherence with invalidation.

Comments: this question contains many aspects of both Part 1 and Part 2. The sequential calculation time and the interprocess communication latency must be explicitly evaluated according to the characteristics of the computation and of the architecture. The parallel program implementation must take the process mapping into account: only for proper values of the critical parameters related to contention, the shared memory access latency can be evaluated as the base latency.

- b) The same with the following variants:

- SMP architecture;
- $N = 16$ processing elements;
- all processing elements integrated on the same CMP, together with a binary generalized fat tree interconnection network, and 4 external memory interfaces;
- 4 external shared memory macro-modules.