Master Program in Computer Science and Networking

High Performance Computing

2012-13

Homework 6

Submit the written answer. Deadline: lecture of November 26 (**Question 1**) and November 28 (**Question 2**), or send an *e*-mail. The work has to be discussed at Question Time.

The answers must be properly and clearly explained.

Question 1

a) Prove that the ideal service time of the Instruction Unit of a scalar pipeline CPU is equal to one clock cycle.

b) Explain how the firmware architecture interprets the following assembler annotations*:*

i) don't_deallocate,

ii) delayed_branch.

That is: explain which unit(s) are involved, which actions are performed, and whether such actions introduce a significant delay.

c) The Instruction Unit of a scalar pipeline CPU executes the instruction GOTO OFFSET. The immediately next instruction *received* by the Instruction Unit might be the instruction at address IC + OFFSET (where IC is the address of GOTO OFFSET): explain why.

d) An assembler machine D-RISC+ contains all the instructions of D-RISC and a further instruction:

ADD_MEM Ra, Rb, Ri, Rc

encoded in one word, with the following semantics:

$$VM[\ RG[a] + RG[i]\ ] + VM[\ RG[b] + RG[i]\ ] \rightarrow RG[c],\ IC + 1 \rightarrow IC$$

1) Modify the D-RISC firmware architecture in order to support this instruction too.

2) Compare the completion time of the vector addition program for two scalar pipeline CPUs: 1) pure D-RISC, 2) D-RISC+.

e) Imagine one or more program segments in which some instructions can be processed in parallel to the data cache fault handling (block transfer) in a pipeline CPU.

Question 2

Evaluate the completion time of a program so defined: operates on an integer x and an integer matrix A[M][M], and returns an integer array C[M], where, $\forall i = 0 \ldots$ M-1, C[i] is equal to number of times that x is an integer multiple of the elements of A[i][∗].

Let p the probability that x is an integer multiple of an element of A.

The primary data cache is on-demand, associative, write-through, with block size σ. The secondary cache is on-chip and contains A. The Execution Unit is pipelined.

Study the problem for different pipeline architectures according to combinations of:

- scalar *vs* 2-way superscalar,
- in-order *vs* FIFO out-of-order.